REMARKS

Claims 3, 11 and 13 have been canceled without prejudice. Applicants respectfully request further examination and reconsideration of the rejections based on the amendments and arguments set forth below.

Claim Objections

Claims 2, 3, 13, and 14 were objected to in the above referenced Office Action with respect to the terms "memory" and "register" as being allegedly a substantial duplicate thereof. The Applicants respectfully disagree with the Examiner's interpretation of the terms "memory" and "register," however, the Applicants have canceled Claims 3 and 13 in order to overcome the objection. As such, the Applicants respectfully request that the above referenced Claim objections be withdrawn.

Claim Rejections - 35 U.S.C. §112

Claims 3 and 13 have been canceled without prejudice and now obviate the cited 35 U.S.C. §112 rejections.

Claim Rejections - 35 U.S.C. §102

The above referenced Office Action rejected Claims 1, 10 and 12 as being allegedly anticipated by U.S. Patent No. 5,371,878 (hereinafter "Coker"). Applicants respectfully traverse.

Independent Claim 1 recites a limitation whereby the virtual microcontroller executes a set of timing code as the microcontroller executes the boot code, as claimed. Therefore, the microcontroller and the virtual microcontroller execute different codes during the booting phase. Independent Claim 1 further recites a limitation whereby the boot code is stored within the microcontroller and at least one portion of the boot code is inaccessible to the virtual microcontroller, as claimed.

Coker discloses a shadow system executing the same software as the target-ECS from system start-up or reset (see Coker, col. 2, lines 56-58). Coker further discloses that the shadow system and the target-ECS function exactly the same except that the shadow system receives data slightly delayed (see Coker, col. 3, lines 13-16). Accordingly, Coker discloses a system whereby the target-ECS and the shadow system execute the same code and have the same data but slightly delayed. Independent Claim 1 distinguishes over Coker by reciting a limitation whereby the virtual microcontroller executes a set of timing code as the microcontroller executes the boot code, as claimed whereas Coker discloses executing the same code.

Moreover, the above referenced Office Action asserts that:

"Interface means 19 connecting the target-ECS and shadow system is used by Coker to transmit I/O data and does not appear to contain any suggestion that instruction code or boot code is transmitted via interface means."

Claim rejection under 35 U.S.C. 102 cannot be based on speculation nor can it be based on obviousness. The fact that a code does not appear to be

transmitted does not necessarily make the code inaccessible, as claimed. A code may not be transmitted but nevertheless be accessible. As such, there is a vast difference between a code not being transmitted and a code being inaccessible, as claimed.

Furthermore, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The cited reference, Coker, as discussed above fails to expressly or inherently disclose the code being inaccessible, as claimed.

Accordingly, Coker fails to either expressly or inherently disclose or suggest each and every element of the recited limitations of independent Claim 1 including the code being inaccessible, as claimed. Therefore, the Applicants respectfully request the withdrawal of the rejection, under 35 U.S.C. 102(b). Independent Claims 10 and 12 recite limitations similar to that of independent Claim 1 and are therefore patentable over the cited reference for the same reasons. As such, allowance of independent Claims 1, 10 and 12 is earnestly solicited.

Claim Rejections - 35 U.S.C. §103

The above referenced Office Action rejected Claims 1-10 and 12-20 as allegedly being unpatentable over U.S. Patent No. 6,202,044 (hereafter "Tzori"). Applicants respectfully traverse.

Independent Claim 1 recites a limitation whereby the virtual microcontroller executes a set of timing code that is timed to take the same number of clock cycles as the microcontroller executes the boot code, as claimed. By definition booting up a system takes place prior to the actual processing by the system, hence prior to actual emulation. Moreover, the microcontroller and the virtual microcontroller execute different codes. The microcontroller executes the boot code as claimed while the virtual microcontroller executes a set of timing code as claimed.

The above referenced Office Action asserts that "Tzori teaches executing timing code to enable the lock-step synchronization, wherein the timing code is timed to take the same number of clock cycles is clearly taught by Tzori by virtue of the method performed by the simulation process and hardware pod". The Applicants respectfully traverse.

Tzori discloses that during the initialization interval the server process retrieves and transmits the logic configuration data from the logic-configuration library to the hardware pod and loads it onto the configurable-logic ICs (see Tzori, col. 9, lines 20-25). Tzori further discloses that "after completing the initialization interval, the simulation process performs a sequence of simulation

cycles" (see Tzori, col. 9, lines 27-29). Tzori, further continues by describing the method and the process after the initialization interval (see Tzori, col. 9, line 31 to col. 11, line 33). Accordingly, reliance of the above referenced Office Action on the method and the process after the initialization interval, described in Tzori, column 9 line 31 to column 11 line 33, is misplaced and of absolutely no relevance because the recited limitations of the claimed invention are directed to the booting up procedure of an ICE system. Moreover, the above referenced Office Action asserts that the limitation of executing a "boot code" is regarded as an obvious detail of implementation as Tzori teaches executing instructions in general. The Applicants respectfully disagree. Assuming arguendo that executing a "boot code" is obvious detail of implementation, it is still of no relevance what so ever because as described above, the cited portion of Tzori is directed to after the initialization interval.

Moreover, the Applicants do not understand the disclosure by Tzori that the server process retrieving and transmitting the logic configuration data from the logic-configuration library to the hardware pod and loading it onto the configurable-logic ICs (see Tzori, col. 9, lines 20-25) to teach or suggest the recited limitations of independent Claim 1 whereby the virtual microcontroller executes a set of timing code that is timed to take the same number of clock cycles as the microcontroller uses to execute the boot code, as claimed.

Furthermore, "to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either

in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP § 2143 - §2143.03 for decisions pertinent to each of these criteria." See MPEP 2100-134.

The above referenced Office Action fails to establish a prima facie evidence in support of the rejection because the rejection, without furnishing any support what so ever, states that:

> "When disengaging the hardware pod to execute a set of boot code, it would be obvious to a person of ordinary skill in the art that Tzori teaches that the simulation process must execute timing code [...] timed to take the same number of clock cycles."

The Applicants respectfully traverse because the microcontroller and a virtual microcontroller may execute the same boot code instead. As such, the fact that a boot code is executed by the microcontroller does not necessitate execution of a timing code by the virtual microcontroller, as claimed.

Moreover, the above referenced Office Action asserts that "Tzori plainly suggests a combination of lock-step synchronization with timing code that allows the microcontroller and virtual processor to optionally disengage from each other." In support of this assertion, the rejection relies on Tzori disclosing that "an

advantage of the improved digital logic simulation/emulation system is that it frees the digital-logic simulation process and the hardware pod from operating in lock-step with each other at the stimulation/response cycle of the digital logic circuit (see Tzori, col. 5, line 64 to col. 6, line 1). Freeing the digital-logic simulation process and the hardware pod from operating in lock-step renders the recited limitation of independent Claim 1 of lock-step synchronization, as claimed inoperable.

Therefore, the above referenced Office Action fails to establish a prima facie evidence in support of the rejection. Accordingly, independent Claim 1 is not rendered obvious, under 35 U.S.C. §103(a), over Tzori. Independent Claims 10 and 12 recite limitations similar to that of independent Claim 1 and are therefore patentable for the same reasons. Dependent Claims 2, 4-9 and 14-20 are patentable by virtue of their dependency.

Moreover, regarding Claims 7 and 18, the above referenced Office Action takes official notice without any support what so ever that "breakpoints are well known in the art" and that "it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to implement breakpoints as known in the art." The Applicants respectfully disagree with this assertion. Applicants respectfully direct the Examiner to MPEP §2144.03(E), which states that "[i]t is never appropriate to rely solely on common knowledge in the art without evidentiary support in the record as the principal evidence upon which a rejection was based." Accordingly, the Applicants respectfully invite the

Examiner to "provide documentary evidence in the next Office action if the rejection is to be maintained. See 37 CFR 1.104(c)(2). The Board [or examiner] must point to some concrete evidence in the record in support of these findings to satisfy the substantial evidence test. If the examiner is relying on personal knowledge to support the finding of what is known in the art, the examiner must provide an affidavit or declaration setting forth specific factual statements and explanation to support the finding. See 37 CFR 1.104(d)(2)." See MPEP 2100-144.

Similarly, regarding Claims 9 and 20, the above referenced Office Action takes official notice without any support what so ever that "removing a breakpoint is well known in the art" and "it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to remove a breakpoint if he no longer wanted execution to break at that instruction." The Applicants respectfully disagree with this assertion and for the reasons mentioned above request that the Examiner kindly provide evidentiary support for this assertion or provide an affidavit or declaration setting forth specific factual statements and explanation to support the finding (see 37 CFR 1.104(d)(2)) if the rejection is to be maintained.

Furthermore, the above referenced Office Action states that Claims 8 and 19 recite combinations of the limitations found in Claims 2-4 and 7; and 13-15 and 18 respectively and are obvious in view of Tzori. The Applicants respectfully disagree because such as assertion partly relies on the official notice noted above for Claim 7 which requires evidentiary support or an affidavit or

declaration setting forth specific factual statements and explanation to support the finding (see 37 CFR 1.104(d)(2)). As such, withdrawal of this rejection is earnestly solicited or if the rejection is to be maintained evidentiary support or an affidavit or declaration setting forth specific factual statements and explanation to support the finding is requested.

Moreover, the above referenced Office Action states that Claim 10 recites combinations of the limitations found in Claims 1, 8 and 9 and are obvious in view of Tzori. The Applicants respectfully disagree because such as assertion partly relies on the official notice of Claim 9 noted above and requires evidentiary support or an affidavit or declaration setting forth specific factual statements and explanation to support the finding (see 37 CFR 1.104(d)(2)). As such, withdrawal of this rejection is earnestly solicited or if the rejection is to be maintained evidentiary support or an affidavit or declaration setting forth specific factual statements and explanation to support the finding is requested.

As such, allowance of Claims 1-2, 4-10, 12 and 14-20 is earnestly solicited.

The above referenced Office Action rejected Claim 21 as being allegedly unpatentable by Tzori in view of "Emulation of the Sparcle Microprocessor with the MIT Virtual Wires Emulation System" by Matthew Dahl et al. (hereinafter "Dahl") and in further view of "A Reconfigurable Logic Machine for Fast Event-

Driven Simulation" by Jerry Bauer et al. (hereinafter "Bauer"). Applicants respectfully traverse.

Dependent Claim 21 is patentable by virtue of its dependency from the independent Claim 12. The Applicants do not understand either Dahl or Bauer to remedy the failures of Tzori as discussed above. As such, Tzori alone or in combination with Dahl and Bauer does not render Claim 21 obvious, under 35 U.S.C. §103(a). As such, allowance of Claim 21 is earnestly solicited.

For the above reasons, the Applicants request reconsideration and withdrawal of the rejections under 35 U.S.C. §112, 35 U.S.C. §102 and 35 U.S.C. §103.

CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-2, 4-10, 12 and 14-21 overcome the rejections of record and, therefore, allowance of Claims 1-2, 4-10, 12 and 14-21 is earnestly solicited.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

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